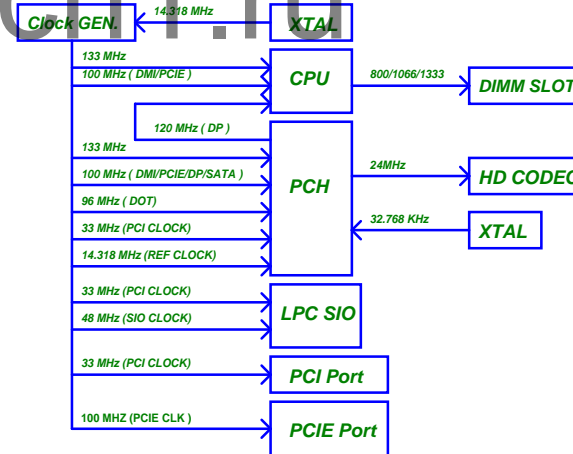
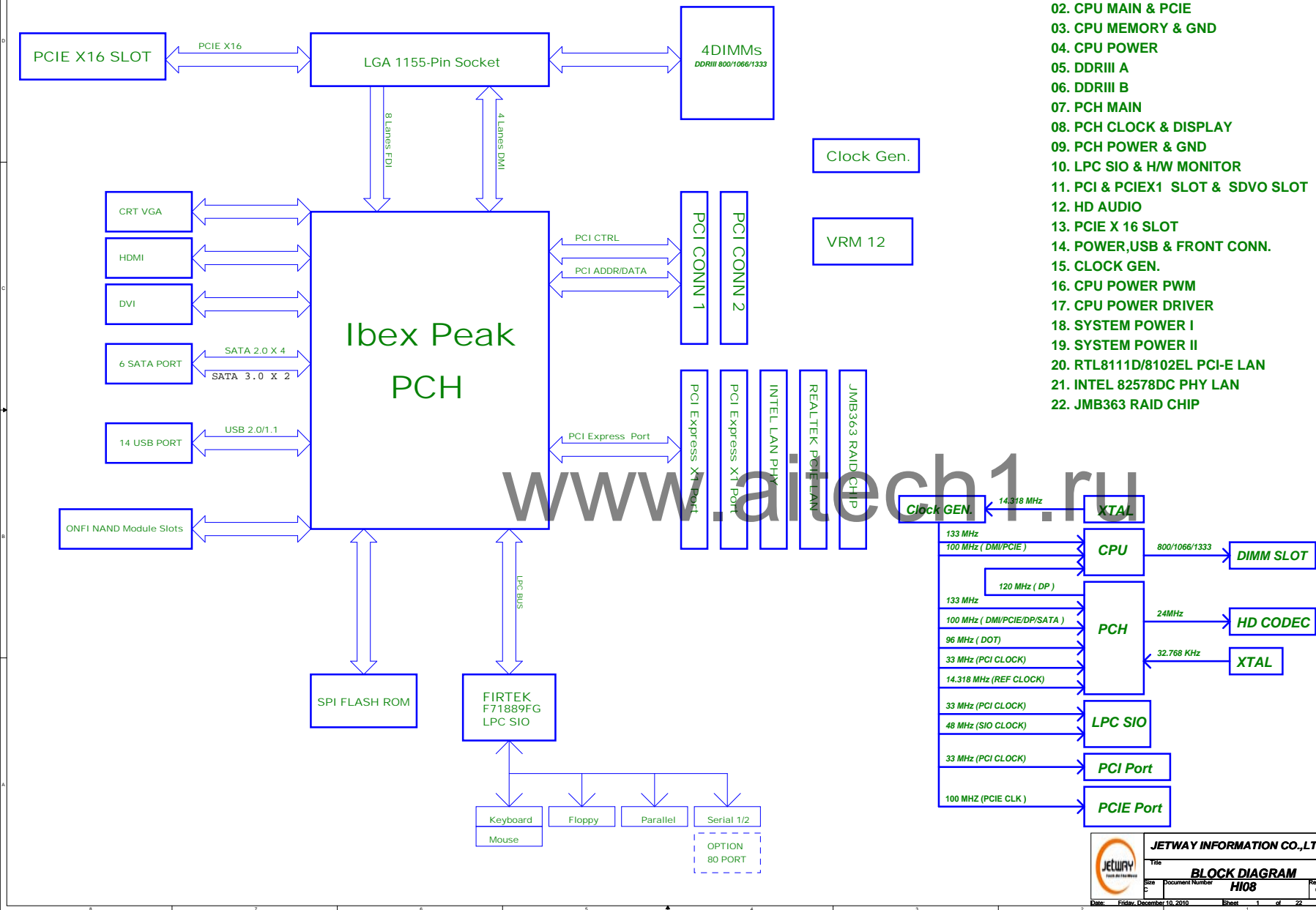
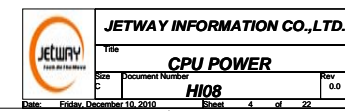


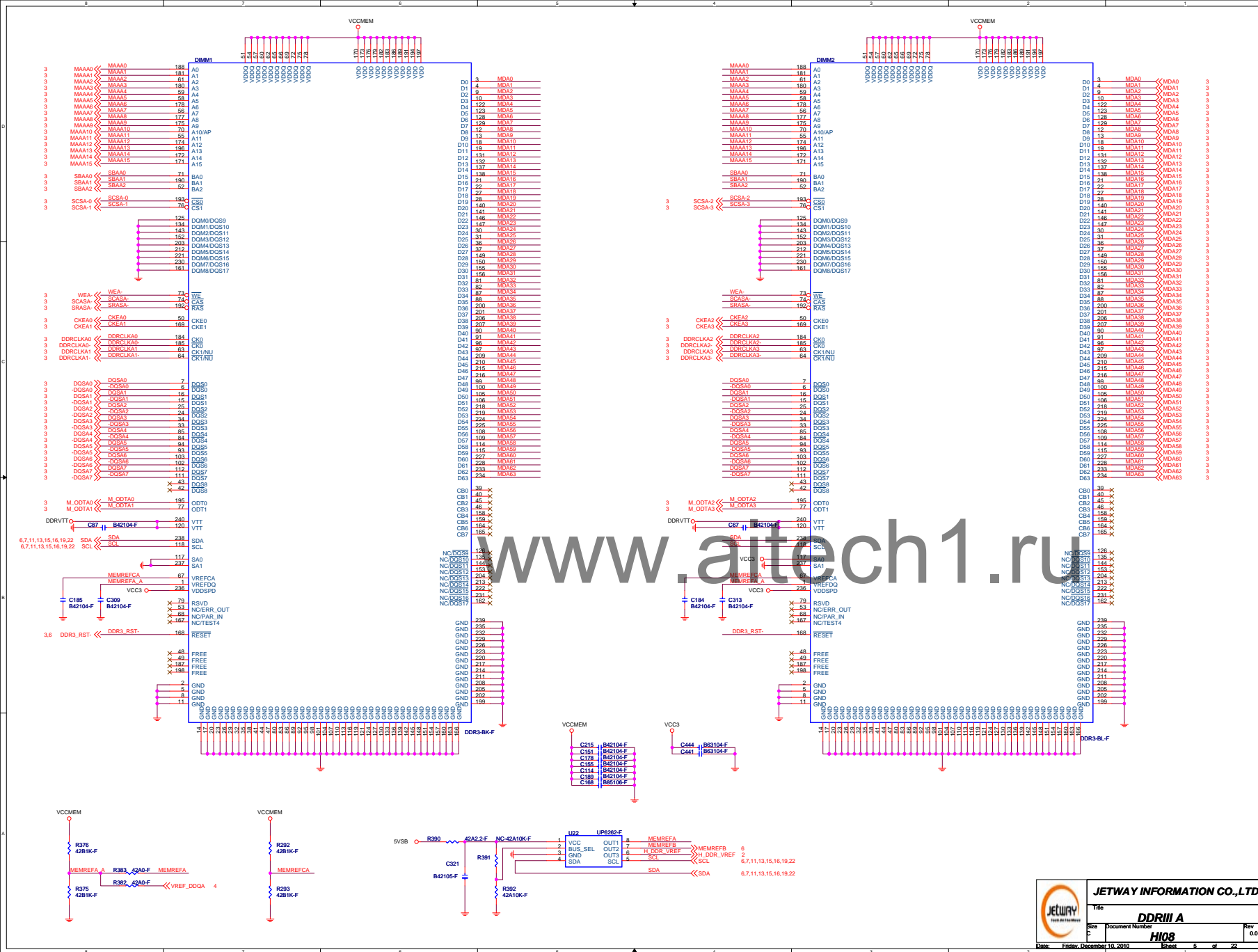
BLOCK DIAGRAM

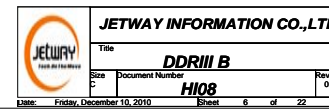
PAGE TITLE

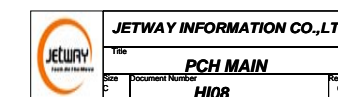
01. BLOCK DIAGRAM
02. CPU MAIN & PCIE
03. CPU MEMORY & GND
04. CPU POWER
05. DDRIII A
06. DDRIII B
07. PCH MAIN
08. PCH CLOCK & DISPLAY
09. PCH POWER & GND
10. LPC SIO & H/W MONITOR
11. PCI & PCIEX1 SLOT & SDVO SLOT
12. HD AUDIO
13. PCIE X 16 SLOT
14. POWER,USB & FRONT CONN.
15. CLOCK GEN.
16. CPU POWER PWM
17. CPU POWER DRIVER
18. SYSTEM POWER I
19. SYSTEM POWER II
20. RTL8111D/8102EL PCI-E LAN
21. INTEL 82578DC PHY LAN
22. JMB363 RAID CHIP

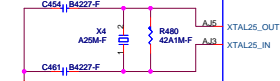
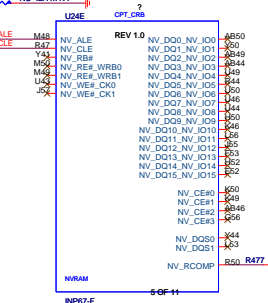





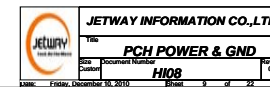






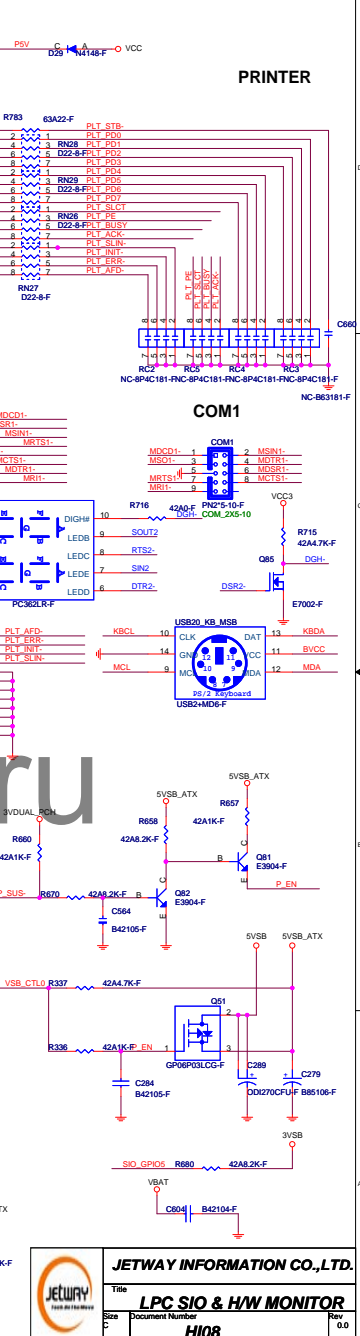
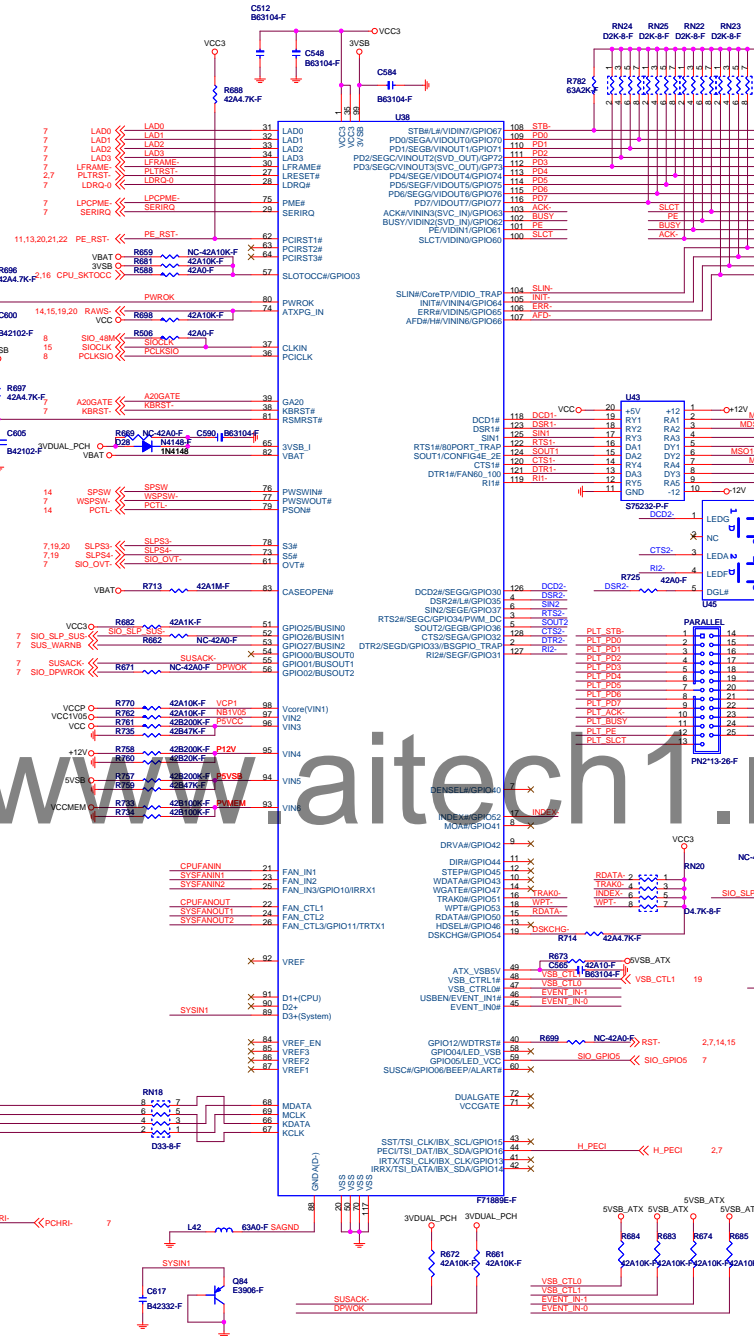
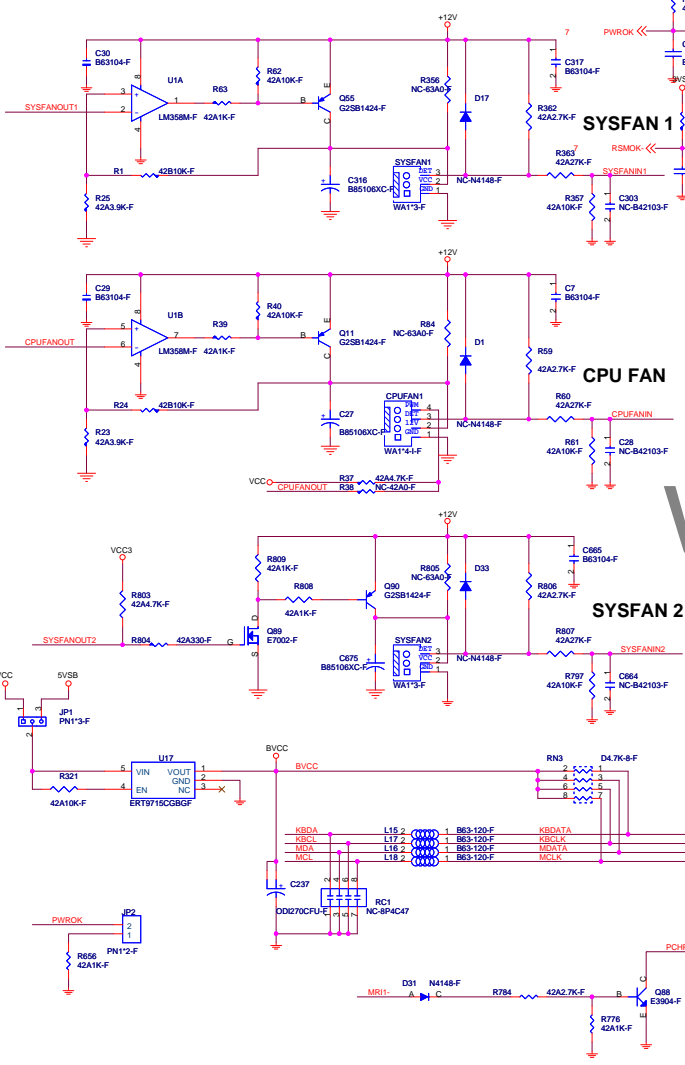


	JETWAY INFORMATION CO., LTD.		
	Title PCH CLOCK & DISPLAY		
	Size C	Document Number H108	Rev 0.0
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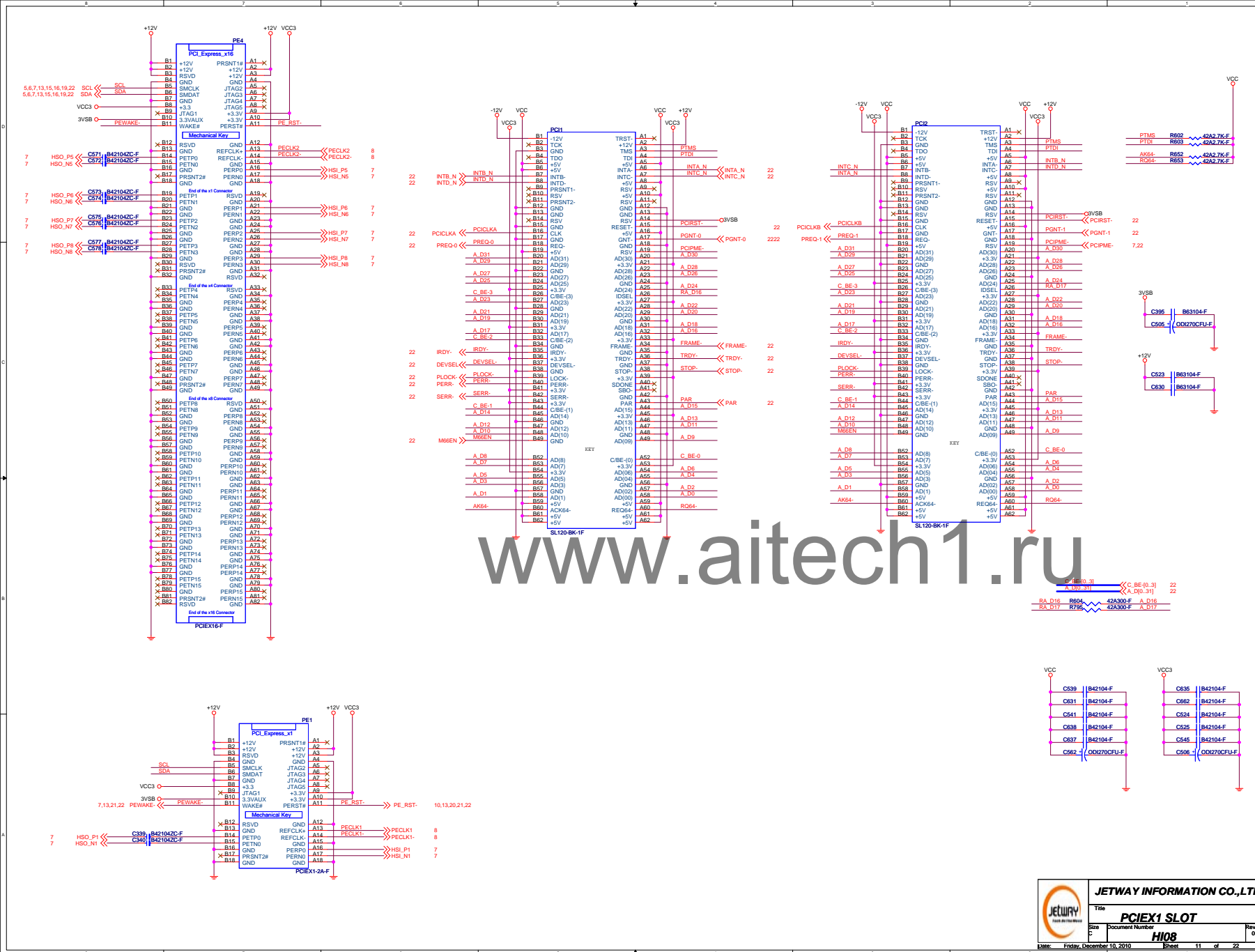


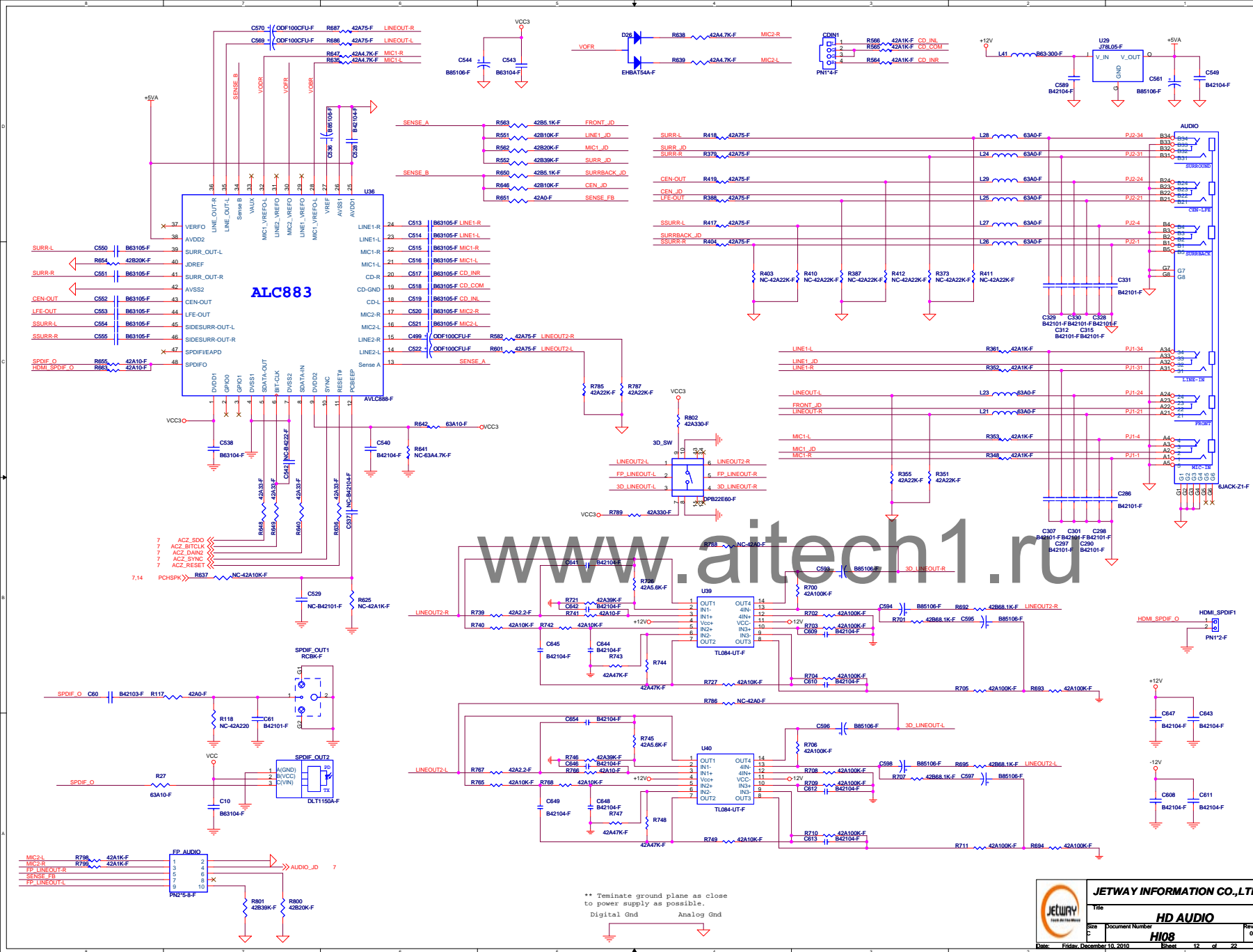
Power On Strapping Options

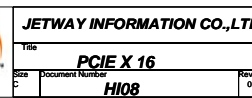
- PIN2 DTR2# HI:SPI as a back up BIOS(Default)
LO:SPI as primary BIOS
- PIN3 RT92# HI:PWM FAN(Default)
LO:DAC FAN
- PIN5 SOUT2 HI:SPI Function Disable.(Default)
LO:SPI Function Enable.
- PIN28 LDRQ# HI:PIN 51-56 are bus Interface(Default)
LO:PIN 51-56 are GPIO pin
- PIN104 SLIN# Pull High 1K Pin 100-116 as LPT Interfaces
Pull High 20K Pin 100-116 as PVID Controller
Pull Down 1K Pin 102/103/111/112 as SVID Controller
Pull Down 47K Pin 100-103 & 105-116 as GPIO Pin
- PIN121 DTR1# HI:FAN default Duty 60%.(Default)
LO:FAN default Duty 100%.
- PIN122 RT91# HI:80 port decode output form COM2 Interface (Default)
LO:Disable the 80 port function.
- PIN124 SOUT1 HI:80 port.(Default)
LO:2E

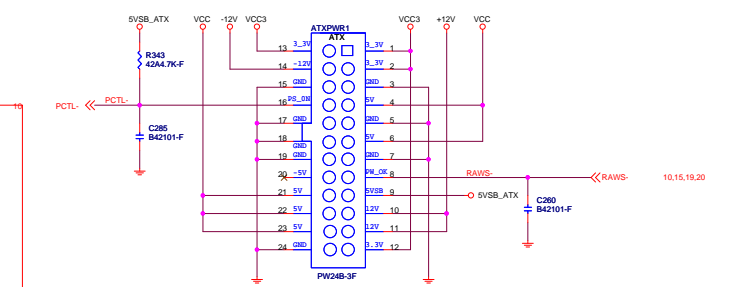
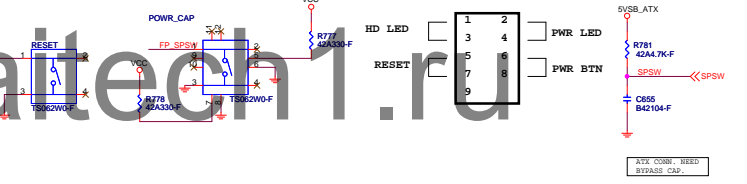
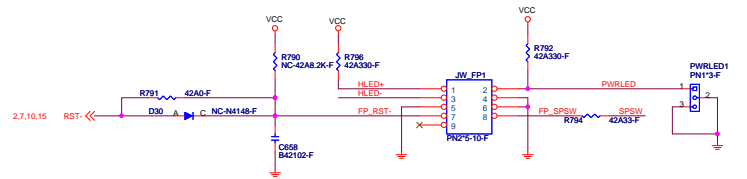
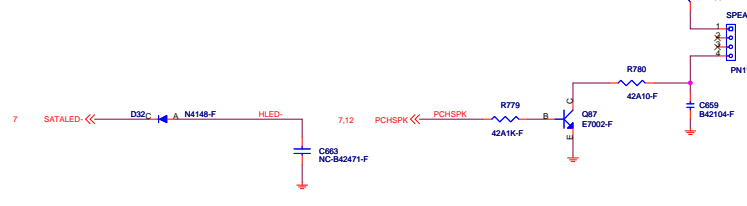
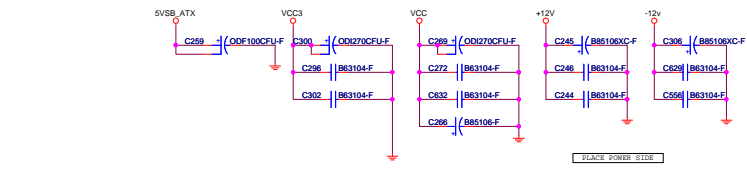
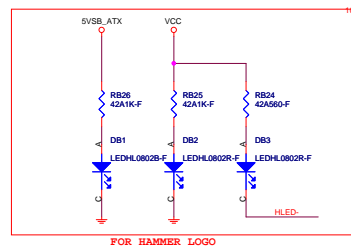
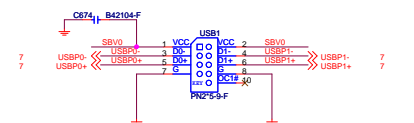
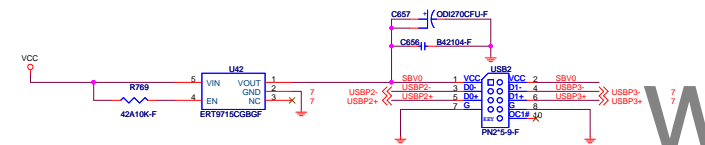
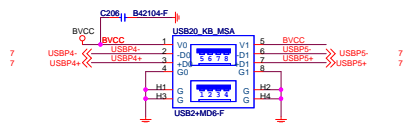
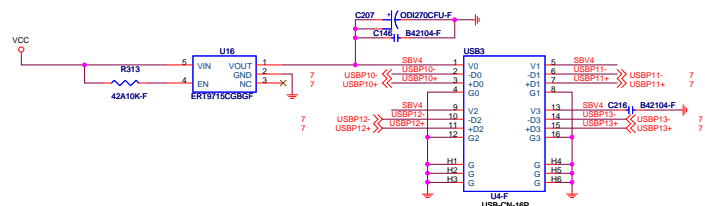
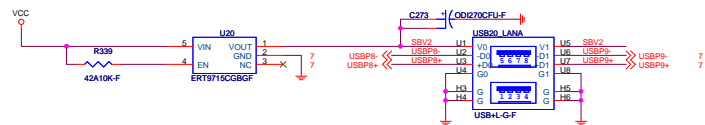


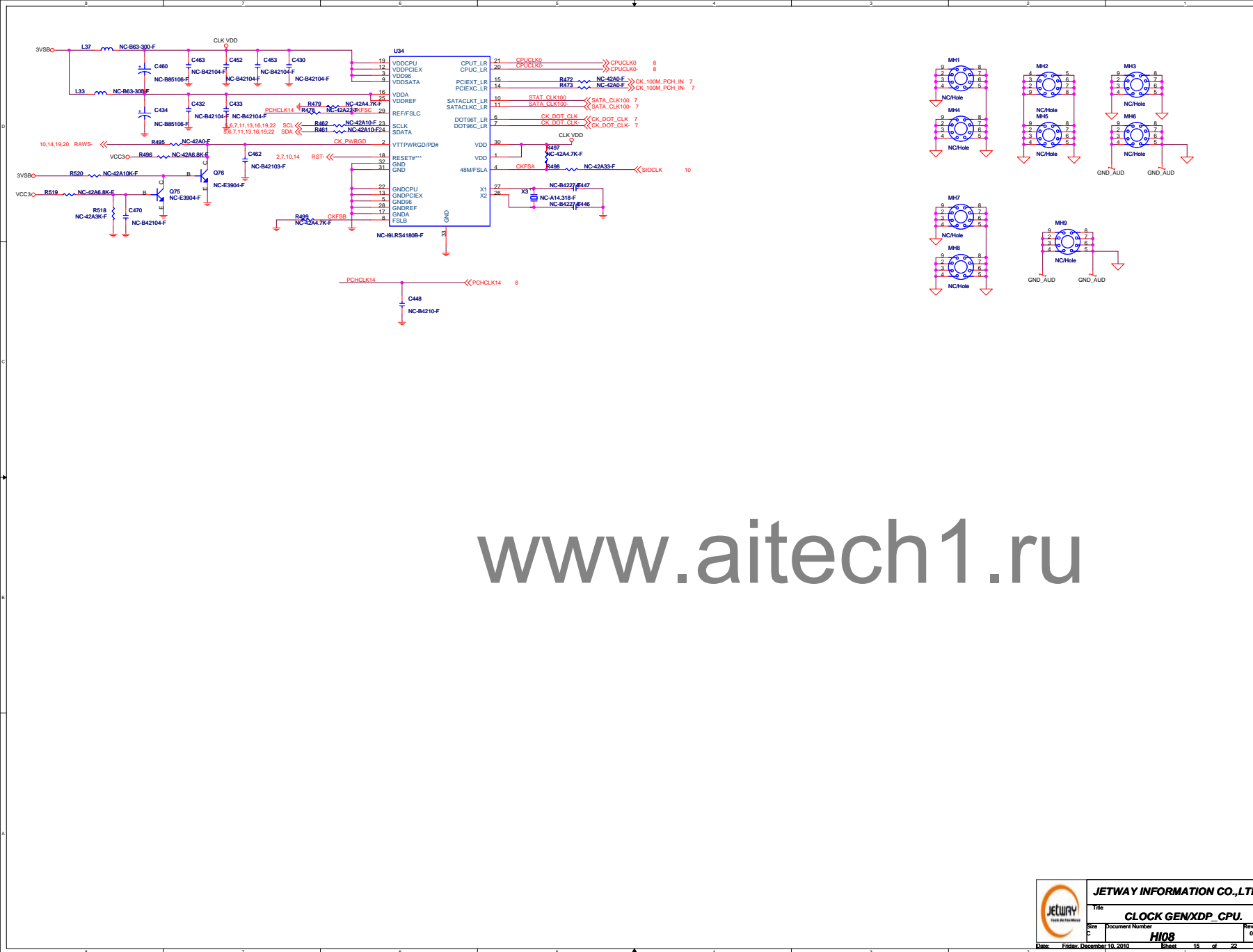
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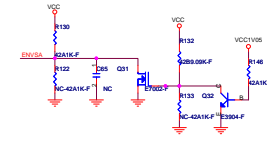
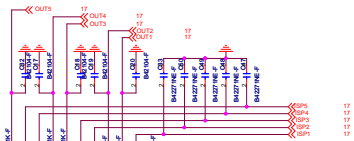
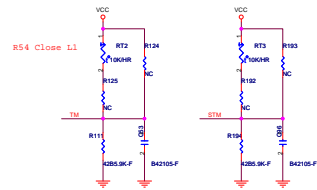
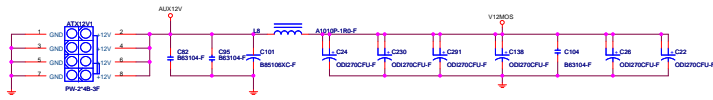


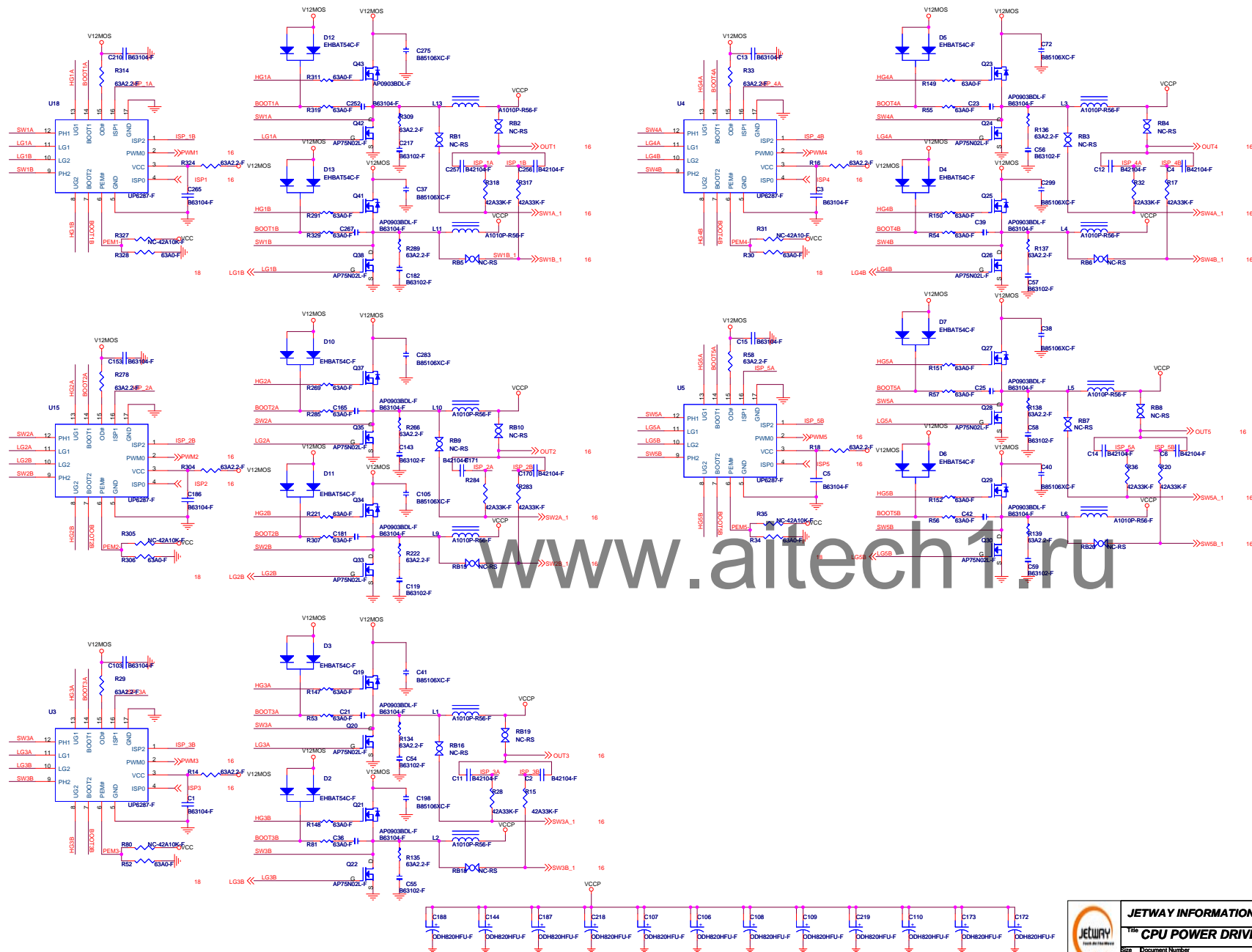


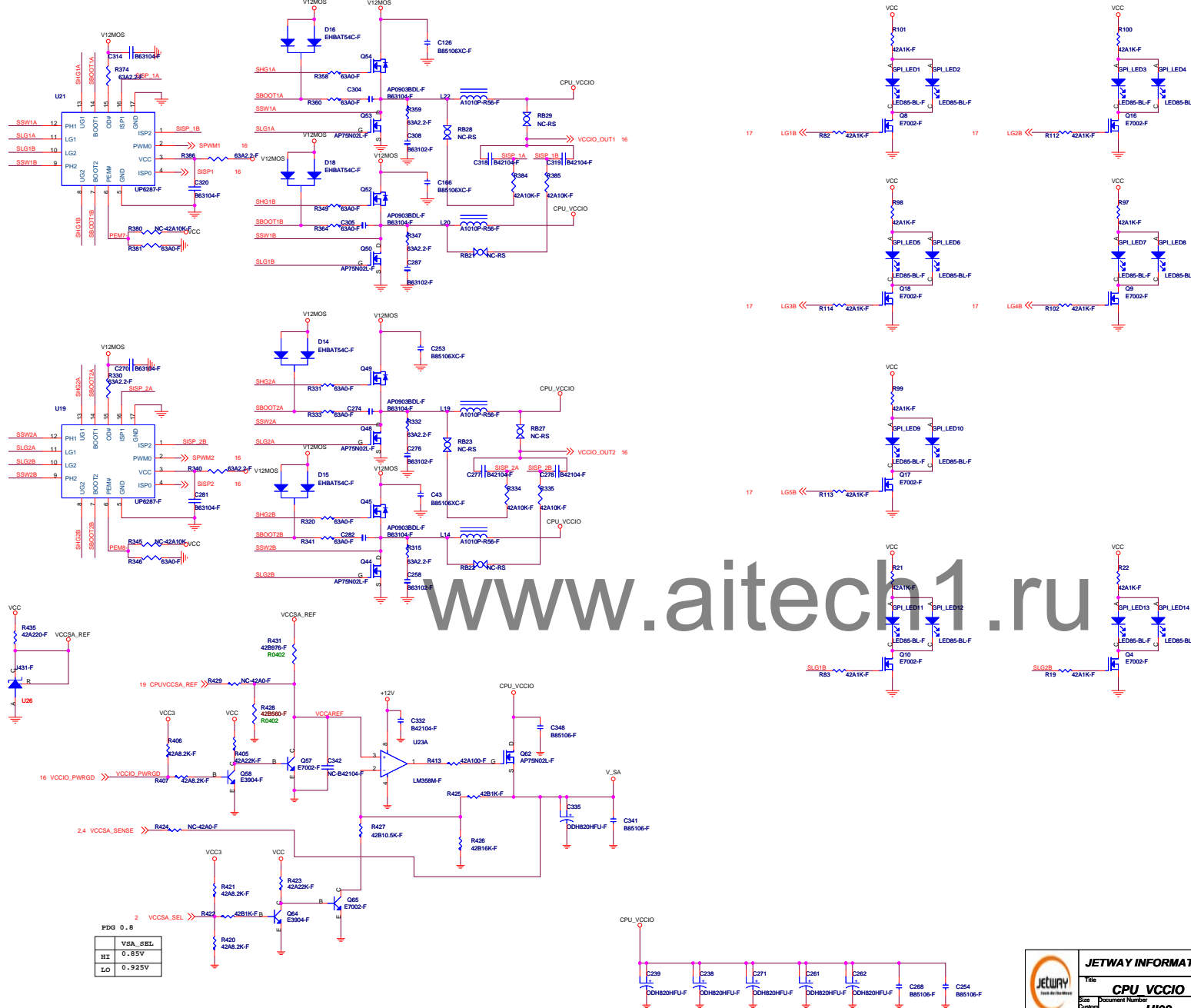


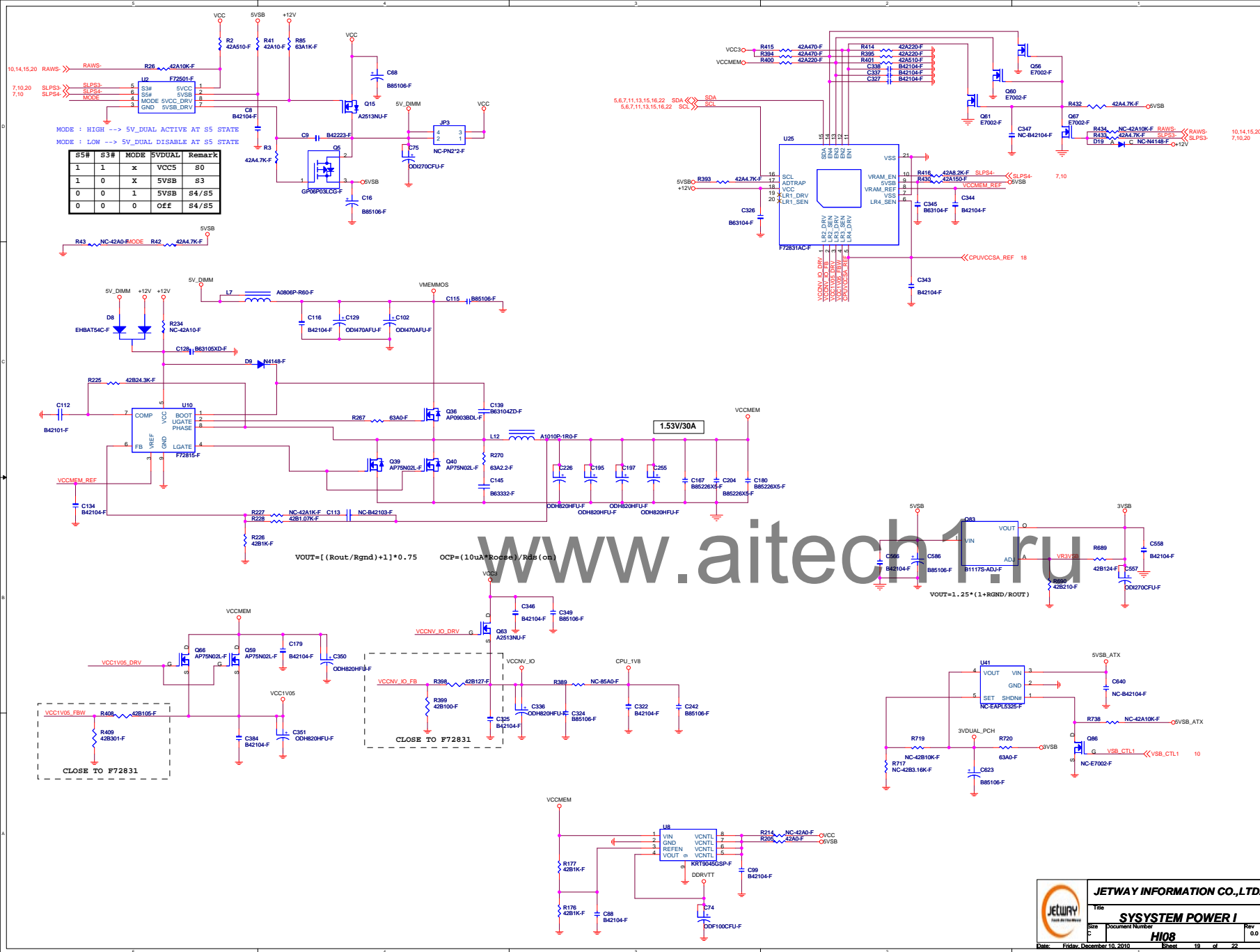


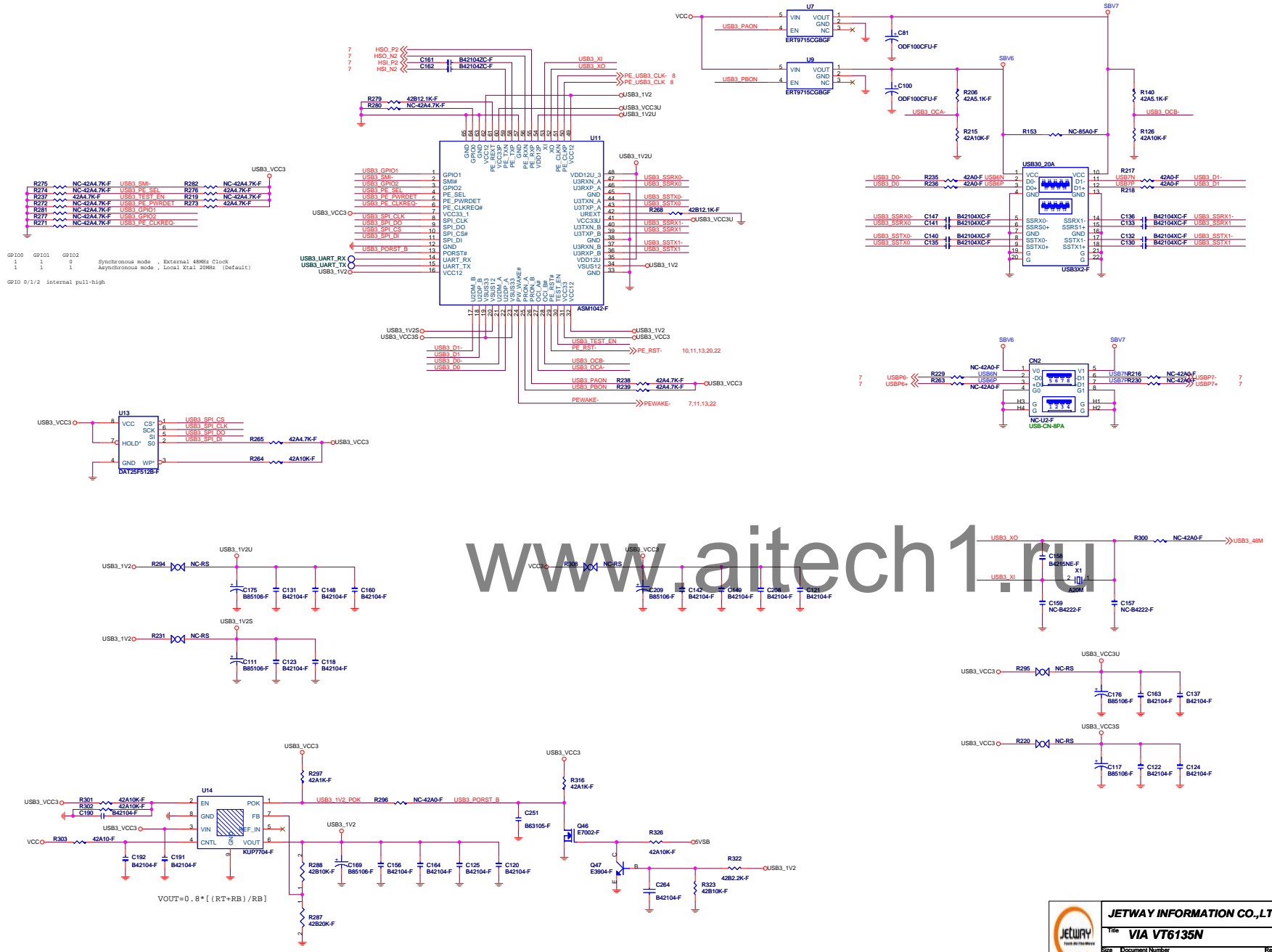


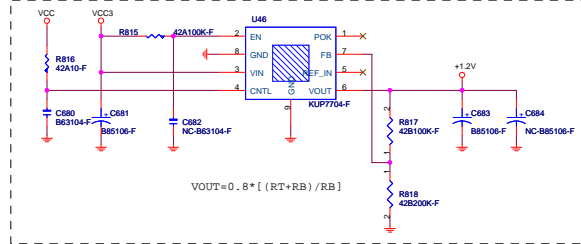
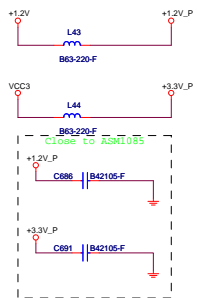
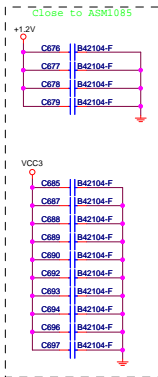












11 PCIRST<< PCIRST

11 PCICLK_A<< PCICLK_B

11 INTA_N<< INTB_N

11 INTD_N<< INTD_N

11 INTD_N<< INTD_N

11 A_D0[3:1]<< FRAME

11 C_BE[0:3]<< FRAME

11 FRAME<< FRAME

11 TRDY<< TRDY

11 TRDY<< TRDY

11 STOP<< STOP

11 DEVSEL<< DEVSEL

11 PLOCK<< PLOCK

11 PREQ-0<< PREQ-0

11 PREQ-1<< PREQ-1

11 PGNT-0<< PGNT-0

11 PGNT-1<< PGNT-1

11 PAR<< PAR

11 PERR<< PERR

11 SERR<< SERR

7,11 PCIPME<< PCIPME

8 ASMPCL_CLK<< PCICLK

CLK100SEL Strapping Set

CLK100SEL	H	L
PCIe CLK	100M +/-N%	100M +/-N%
PCICLK_IN	X	33M
PCICLK_O	33M +/-N%	33M

PE_EC_SEL-

"H" for Express Card mode

"L" for PCIe Riser Card mode

CLK100SEL-

"H" for PECLK input only

"L" for PECLK & PCICLK input

TEST_EN-

"H" for Test Mode Enable

"L" for Test Mode Disable

-CLKRUN_EN-

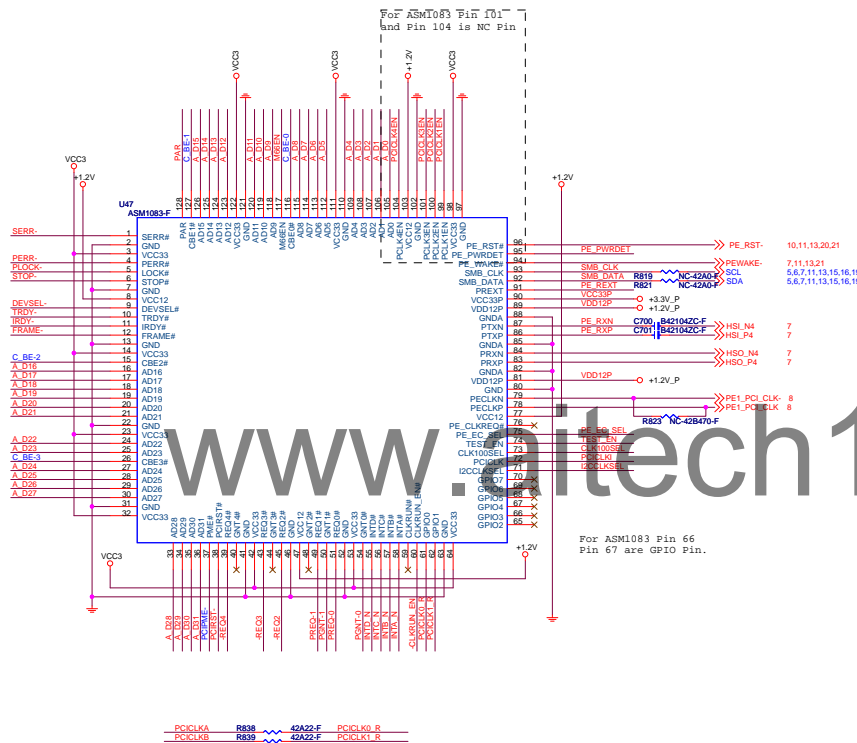
"H" for CLKRUN Mode Disable

"L" for CLKRUN Mode Enable

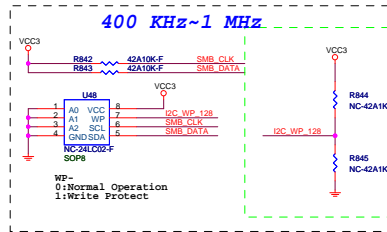
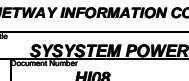
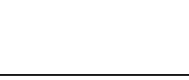
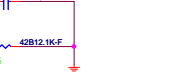
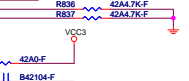
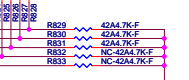
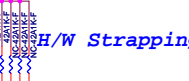
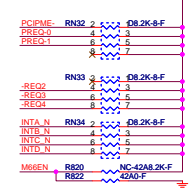
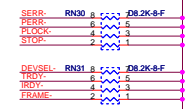
I2CCLKSEL-

"H" is 135KHz I2CCLK

"L" is 67.5KHz I2CCLK



For ASM1083 Pin 66
Pin 67 are GPIO Pin.



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Title: **SYSYSTEM POWER I**

Doc: **H108**

Rev: **0.0**

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